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EXAMINER	
HORNING, JOEL G	
ART UNIT	**PAPER NUMBER**
1712	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	**Application No.**	**Applicant(s)**	
	10/552,681	MEIER ET AL.	
	Examiner	**Art Unit**	
	JOEL G. HORNING	1712	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,14-23 and 25-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,14-23 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. In the response of March 22nd, 2010, applicant has: amended claims 12, 23, 27 and 29 and cancelled claim 24. Claims 12 and 14-29 are currently pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 22nd, 2010 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 12, 15, 17, 19, 26 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692).

Wojnarowski et al is directed towards a manufacturing method for patterning polymer layers in a multiple layer electronic device (abstract), such as circuit interconnect devices (col 1, lines 8-10), which sense electrical potentials placed on their metal traces by sending an electrical signal, which can be read, thus they can be considered "test sensor" devices. As shown in figures 3a-d, the method comprises supplying a substrate **10** with a metallic layer (chip pad) **17** deposited on it, onto which an intermediate bilayer **18** and **20** is deposited, onto which a hard mask layer of a dielectric material (which is also not intended to conduct electricity: non-conducting layer. e.g. silicon nitride) **76** is deposited via plasma enhanced CVD (col 7, lines 38-56). A portion of the intermediate layer (along with the corresponding portion of the non-conductive layer) is then removed by applying laser energy to the intermediate layer (**claim 26,** col 7, lines 57-63). This section does not teach whether the laser was energetic enough to ablate the silicon nitride masking material as well as the underlying dielectric material. However, Wojnarowski teaches several different ways to remove the masking and dielectric material layers, including an embodiment where the masking material is not very absorbing to the laser light, while the underlying dielectric is very absorbing to the laser light, so that the laser ablates the underlying dielectric layer and the ablated dielectric material causes the removal of the masking material above it (col 3, lines 37-48).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to use this embodiment of Wojnarowski, where the laser ablates the polymer layer (sacrificial layer), which causes the removal of the non-conductive layer above it because it was a taught method to perform the patterning of the layers which would produce predictable results.

Wojnarowski et al does not teach how the contact pad **17** is formed.

However, Lee et al teaches that metal contact pads are conventionally formed by sputtering methods (a physical vapor deposition process) [0072].

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to deposit the contact pads by physical vapor deposition (sputtering) since it was known to the art to be the conventional method of depositing such pads and would produce predictable results **(claim 12)**.

4. Regarding **claim 15**, Wojnarowski et al teaches further removal of the intermediate layer by using an ion beam (reactive ion etch, which uses a beam of ions) (col 7, lines 64-67 which directs to col 5, lines 42-43).
5. Regarding **claim 17**, Wojnarowski et al teaches that the metal contact can be aluminum (col 6, lines 36-40).
6. Regarding **claims 19 and 27**, Wojnarowski et al teaches making the intermediate sacrificial layer of polytetrafluoroethylene (C_xF_y), either with an additional polyimide layer (col 5, lines 54-55) or by itself (col 8 line 65 through col 9, line 3).

7. **Claims 14, 16 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692) further in view of Janai et al (US 6255718).

As discussed previously, Wojnarowski et al in view of Lee et al teaches depositing a layered structure with a polymer intermediate layer (e.g. fluoropolymers like PTFE) over the metal contacts and then patterning it by laser ablation. It further teaches depositing the polymer intermediate layer in the form of a liquid or a laminate (col 5, lines 14-26), but it does not teach depositing them by PECVD.

However, Janai et al is also directed towards the deposition of polymer layers and then patterning those polymer layers through laser ablation in order to create electronic devices (abstract). Since the polymer layer can be built of fluorocarbon monomers, it also teaches forming these polymer layers as fluoropolymers (col 4, lines 20-21). It further teaches that it is known to deposit these polymer layers by other methods such as liquid deposition methods, but that most polymers deposited this way are transparent to visible light and thus require expensive and less efficient UV lasers in order to ablate them (col 2, lines 23-32). In order to overcome this, it teaches depositing the polymer layers by a PECVD process, which can then allow the polymers to be ablated by visible light lasers (col 3, lines 19-34), they further teach that by modifying the polymer deposition process, the laser absorption of the polymer layers can be tailored for any chosen lasers wavelength (col 7, lines 21-26).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to deposit the fluoropolymer intermediate layers of Wojnarowski et

al in view of Lee et al by the PECVD process of Janai et al in order to be able to ablate the polymer layers with less expensive visible light lasers and to be able to tailor the absorption of the polymer to match available lasers instead of buying a laser of the proper frequency for different polymeric materials **(claim 20)**.

8. Regarding **claim 14**, Wojnarowski et al in view of Lee et al, does not teach what energy densities are required to ablate their polymer intermediate layers, however, Janai et al teaches ablating the polymer layers with a relatively small amount of laser energy (col 1, lines 42-45) and teaches that its plasma deposited polymers can be ablated at energy densities less than $4J/cm^2$, which overlaps with applicant's claimed range (col 5, lines 62-64).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to use the energy densities taught by Janai et al to ablate the plasma deposited polymer intermediate layers, since they are taught to be suitable for those layers.

MPEP 2144.05 states: "In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists."

9. Regarding **claim 16**, Wojnarowski et al in view of Lee et al does not teach if their polymer intermediate layers can be ablated by electron beams, but Janai et al teaches that plasma deposited polymers can be ablated by electron beams (col 4, lines 24).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to ablate some of the polymer intermediate layer material though

electron beams since it was known to be a suitable method for ablating such plasma deposited polymer layers and would produce predictable results.

10. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692) further in view of Trapp et al (US 2002/0192976).

As previously discussed, Wojnarowski et al in view of Lee et al teaches the deposition of an electrically non-conductive (e.g. SiN) layer as an etching masking layer, but it does not teach how thick the layer should be.

However, Trapp et al is also directed towards the formation of etching mask layers and teaches that the thickness of masking layers should be adjusted so that it is thick enough to prevent undesired etching of the substrate, yet thin enough not to hinder the etching process for the desired feature size [0050]. Put another way the thickness of the non-conductive layer is a result effective variable for avoiding undesired etching conditions.

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to choose the instantly claimed ranges of “a thickness less than or substantially equal to 1 micon” through process optimization, since it has been held that when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. See In re Boesch, 205 USPQ 215 (CCPA 1980).

11. **Claims 21 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692) further in view of Young (US 2002/0139981).

Wojnarowski et al in view of Lee et al teaches that the "substrate **10** may comprise any structural material" (col 4, lines 65-66), which would include using a polymeric or flexible material, but it does not specifically teach doing so.

However, Young is also directed towards the formation of electrical devices (which include interconnect devices) and it teaches that flexible polymer substrates (such as polyimide [0024]) are desirable substrates for the formation of semiconductor circuit elements since they are flexible, which means they can be used to make curved devices or rolled up to save space or so the device can be formed into other aesthetically pleasing shapes [0002].

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to use a flexible polymer substrate as the substrate in the process of Wojnarowski et al in order to be able to produce non-planar electrical devices for aesthetic or design reasons or to have a devices which can be rolled up in order to save space **(claims 21 and 22)**.

12. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692) further in view of Owen (US 5593606).

Wojnarowski teaches alternately depositing and using a conductive metallic layer as the hard masking layer (which is on top of the sacrificial layer) instead of the

non-conducting ceramic layer (e.g. silicon nitride, col 8, lines 45-50). Wojnarowski does not explicitly teach using multiple masking layers in order to pattern its electrical interconnect circuits (col 1, lines 5-15).

Owen is also directed towards electrical interconnect circuits comprising layers of metals, polymeric dielectrics (e.g. PTFE) and ceramic layers (col 1, lines 15-46) which are machined by ablating the layer materials with a laser system (col 2, lines 39-46). However, Owen furthermore teaches that these multilayer interconnect multilayer structures (such as those made by Wojnarowski) are additionally stacked on each other forming more complicated interconnect structures (col 1, lines 46-49).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to perform the process of Wojnarowski in view of Lee described for claim 12 several times on different subsections in the stack, and additionally when masking layers that are removed by ablating sacrificial layers in the stack include *both* non-conductive layers and metallic layers (i.e. second metallic layer), since it is known to stack such interconnect layers together in order to form a desired interconnect structure and non-conductive and metallic mask layers are both taught for that use, so it is obvious to use both **(claim 23)**.

13. **Claim 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692) further in view of Young (US 2002/0139981) further view of Polak (US 4382101).

Wojnarowski et al in view of Lee et al further in view of Young et al does not teach plasma treating the polymer substrate before depositing the metal layer.

However, Polak is also directed to metal clad polymers (for example, polyimide, column 1, lines 60-65) and teaches that by plasma treating (a plasma activation process) polymer substrates before depositing the metal, the peel strength of the metal layer can be increased (abstract).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to perform a plasma activation (plasma treatment) on the polymeric substrate (such as the polyimide taught by Young and Polak) before depositing the metal layer in order to increase the peel strength of the metal layer and thus have a more robust structure.

14. **Claims 28 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wojnarowski et al (US 5302547) in view of Lee et al (US 2002/0121692) further in view of Hanyu et al (US 5876877) in view of Yamada et al (US 5319479).

Wojnarowski et al in view of Lee et al teaches using an optically transparent mask layer (e.g. SiN) through which the dithering laser is passed during ablation and which provides protection to the underlying areas during the etching process (col 7, lines 43-63) over the intermediate sacrificial layer. This mask layer can be nitrides or oxides (col 8, lines 45-50), but Wojnarowski et al does not specifically teach using a ceramic layer comprising MgO as this mask layer.

However, Hanyu et al is also directed towards mask layers which are required to be optically transparent to the optical beams used and yet protect the underlying areas during conventional etching processes (act as an etch stop). It teaches that layers comprising of MgO are suitable for such layers (abstract). It further teaches

that SiN is conventionally used for such layers, but that as the laser wavelengths used for patterning become smaller the laser absorption of these layers becomes larger than is desirable (col 1, line 52 through col 2, line 17), so it teaches instead using ceramic mask layers comprising Al_2O_3-MgO (which is considered insulating or "non-conductive") because they are more suitable for these lower wavelength laser patterning processes (col 3, line 57 through col 4, line 6). However, Hanyu et al only teaches depositing the Al_2O_3-MgO film by an ion beam assisted electron beam source (col 4, lines 9-14).

However, Yamada et al is also directed towards the formation of multilayer electronic devices (abstract) and it teaches that Al_2O_3 and MgO are both suitably deposited onto polymers by using Plasma enhanced CVD (col 4, lines 9-18).

Thus it would have been obvious to a person of ordinary skill in the art at the time of invention to use a non-conductive ceramic layer comprising MgO as the masking layer instead of SiN because the MgO ceramic is taught to provide superior optical transparency at lower laser wavelengths while still providing a suitable amount of masking protection and to deposit the layer by plasma enhanced CVD since it was a method known to be suitable for depositing those materials onto polymeric surfaces for electronic applications **(claims 28 and 29).**

Response to Arguments

15. Applicant's arguments with respect to **claims 12 and 14-29** have been considered but are not convincing in view of the new ground(s) of rejection necessitated by amendment.

16. Regarding applicants arguments directed towards **claim 12**, though the previous basis for rejection was overcome, upon further review of the Wojnarowski reference, the examiner determined that Wojnarowski specifically teaches an embodiment of using a sacrificial layer to remove the non-conductive layer on top of it, as claimed by applicant.

Conclusion

No current claims are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOEL G. HORNING whose telephone number is (571) 270-5357. The examiner can normally be reached on M-F 9-5pm with alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael B. Cleveland can be reached on (571)272-1418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. G. H./
Examiner, Art Unit 1712

/David Turocy/
Primary Examiner, Art Unit 1715